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09/977,994	10/17/2001	Makoto Nagata	50006-128	4496

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EXAMINER	
WEST, JEFFREY R	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/977,994	Applicant(s) NAGATA ET AL.
	Examiner Jeffrey R. West	Art Unit 2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. In claims 2 and 9, "wherein where the digital circuit" should be —wherein the digital circuit—.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment" in view of Shimazaki et al., "LEMINGS: LSI's EMI-Noise Analysis with Gate Level Simulator".

Nagata discloses a method for performing measurements and analyses of substrate noise waveform in mixed signal integrated circuit environment comprising representing the integrated circuit according to a distribution of switching operations of a plurality of logic gates and a time series of statically-charged parasitic capacitors connected between a source line and a ground line (page 577, column 1, paragraph 5 and Figure 7). Nagata then discloses generating an analysis module by coupling one end of the group of capacitors with a parasitic impedance of the source line, and

connecting the other end of the group of capacitors with a parasitic impedance of the ground line (Figure 7). Nagata also discloses that the source current from the analysis model along with the parasitic impedances of the source and ground lines causes a voltage variation, regarded as substrate noise (page 576, column 1, paragraph 3, page 577, column 1, paragraph 4, and Figure 5). Nagata further discloses that a value for the parasitic capacitances is determined every predetermined time interval wherein the time interval is set according to the switching operations of the logic gates (page 577, column 2, paragraph 2 to page 578, column 2, paragraph 2). Also, although not specifically disclosed, it is considered inherent that the time interval is shorter as the frequency of the switching operations is greater since frequency and time have an inverse relationship.

With respect to claims 2 and 9, Nagata discloses assigning the group of parasitic capacitors to a group of logic gates wherein the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally appended (i.e. increased) (Figures 7a-c and page 577, column 2, paragraph 2).

With respect to claims 5 and 12, Nagata discloses that the capacitance of the parasitic capacitor to be charged is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed (page 577, column 2, paragraph 2 and equation (2)) (input capacitances, $C_{In,i}$ and $C_{Ip,j}$, and output capacitances $C_{jn,i}$ and $C_{jp,j}$).

Nagata, however, presents the voltage variation as a measure of noise and doesn't specifically disclose determining the waveform of the source current in the digital circuit from the analysis model.

Shimazaki teaches a method for noise analysis comprising determining the noise of an integrated circuit by creating a gate-level simulation of the integrated circuit (2.1) and from it determining an estimate current waveform for noise analysis (2.3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata to include determining the waveform of the source current in the digital circuit from the analysis model, as taught by Shimazaki, because, as suggested by Shimazaki, the combination would have provided a means for conveniently determining the EMI noise characteristics from the current waveform in a time-reducing method (2.6 and 2.7).

Further, Applicant admits as well known in the art, in the Background of the Invention, that "the principal cause of substrate noise generation is a change in voltage generated when the source current of the digital circuits flowing through internal power-supply and ground wirings, which connect the external power supply to the LSI chip, interacts with the parasitic impedances parasitic on those wirings" (page 2, lines 15-20) and "As clearly understood, the generation of noises largely depends on a change in the source current" (page 3, lines 1-2). *When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejections. In re Nomiya, 509 F.2d 566, 184 USPQ 607, 610 (CCPA 1975).*

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. in view of Shimazaki et al. and further in view of Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in WRIGHT".

As noted above, the invention of Nagata and Shimazaki teaches many of the features of the claimed invention including performing noise analysis on previously designed circuit as well as suggesting that the current analysis method can aid designers in integrated circuit quality (Shimazaki et al., abstract) but does not specifically disclose the method for designing the semiconductor integrated circuit comprising receiving the design information, designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis.

Mitra teaches a computer-implemented method for handing substrate-coupled switching noise in a typical IC containing both sensitive analog and noisy digital circuits (abstract) comprising first receiving minimal area and wire length design specifications, designing the circuits based on the design specifications, and from the design determining the current substrate noise. Mitra then teaches re-designing, based on the substrate noise results, the circuits and guard ring/band positions to obtain acceptable substrate noise results (page 275, column 2, paragraph 3 to page 276, column 1, paragraph 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata and Shimazaki to include a method for designing the semiconductor integrated circuit comprising receiving the design information, designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis, as taught by Mitra, because, as suggested by Mitra, the combination would have provided a method for incorporating a simplified switching noise estimation into a simulated annealing placement algorithm to allow substrate design that can be used during the design wherein efficient evaluation is critical, but much information about the final chip remains unavailable (page 277, column 1).

Response to Arguments

5. Applicant's arguments filed 03 April 2003 have been fully considered but they are not persuasive.

Applicant argues, "Nagata et al. does **not disclose a parasitic capacitor series including parasitic capacitors to be charged in time series**, recited in claims 1, 6 and 8, and the Examiner did **not point out** where in Nagata et al. those capacitors are disclosed." Applicant then admits that "[w]hat Nagata et al. discloses are parasitic capacitors to be charged or discharged and parasitic capacitors in a stable charged state at a certain instant."

First, the Examiner contends that claims 1, 6, and 8 only require that the digital circuit be represented "as a parasitic capacitor series which is a time series of parasitic capacitors each connected between a source line and a ground line to be charged." Stated in this way, the claim does not require that the capacitors be charged in time series (i.e. in chronological order) but could be broadly interpreted as parasitic capacitors connected in series (i.e. a time series) that are to be charged. In this way, Nagata discloses, in Figure 7, that the parasitic capacitors C_{jp} and C_{jn} are connected in series and are to be charged, thereby meeting the claimed limitations.

Secondly, the Examiner agrees with Applicant's interpretation of Figure 7 showing parasitic capacitors to be charged or discharged (i.e. C_{jp} and C_{jn}) as well as parasitic capacitors in a stable charged state at a certain instant (i.e. C_w, C_{lp}, and C_{ln}). Therefore, Nagata does disclose representing the digital circuit as a parasitic capacitor series and a group of parasitic capacitors each charged statically. With respect to the remaining limitations of claims 1 and 8, (i.e. representing the digital circuit according to a distribution of switching operations of the logic gates in the digital circuit and specifying that the parasitic capacitor be a time series) Figure 7 also indicates that the state of parasitic capacitors C_{jp} and C_{jn} are contingent on the switching operations of the logic gates (i.e. L). Further, it is considered inherent that the parasitic capacitors C_{jp} and C_{jn} must be charged in a time series for the following reason. On page 577, column 1, paragraph 5, Nagata discloses controlling the

switching action to charge or discharge the capacitors according to a truth table. A truth table is well known in the art to be a table listing of all possible combinations of inputs and the corresponding output of a Boolean function. Therefore, in an initial condition, the logic gate would control both switches to be closed, thereby creating a short circuit and not charging either of the capacitors C_{jp} or C_{jn}. Then, the logic gate implementing the second condition of the truth table would control the top switch to be closed and the bottom switch to be open, thereby charging C_{jn} not C_{jp}. The next truth table combination would then open the top switch and close the bottom switch charging C_{jp} not C_{jn}. In this way the parasitic capacitors are charged in series.

Applicant then argues that "there is no motivation to modify the teaching of Nagata et al. based on that of Shimazaki et al. to arrive at the claimed invention." Applicant first argues that Nagata et al. is silent as to "determining the EMI noise characteristics" and as to the "time-reducing" aspects. This is so because Nagata et al. describes that its purpose is "for experimental studies on substrate noise properties in a mixed signal IC environment." The Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, but the motivation need not come from the primary reference itself. Both the inventions of Nagata and Shimazaki are drawn to the same problem of analyzing noise---Nagata of analyzing substrate noise due to VLSI/LSI design, and Shimazaki as noise due to LSI's. As

noted above, the combination would have provided a method for performing a wide variety of noise analysis including a time reducing method for determining the EMI noise characteristics of the LSI design.

Further, while the invention of Nagata discloses analyzing the output waveform as a voltage waveform rather than a current waveform as claimed, it is well known in the art that voltage and current have a direct relationship, and therefore one having ordinary skill in the art would understand that analysis of the two types of waveforms would produce functionally equivalent results.

Applicant then argues that one aspect of the claimed invention is to analyze "the waveform of a source current at an enhanced accuracy and higher speed with consideration of re-distribution of charges through the digital circuit" and "[n]either Nagata et al. nor Shimazaki et al **disclose** this aspect. Applicants submit that without this aspect, one skill in the art would not have been motivated to modify the prior art." The Examiner contends that this purpose cited above is not present in the claimed invention and while the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner also contends that containing an intended purpose or use is not criterion for motivation to modify the prior art.

Finally, Applicant submits that the assertion made by the Examiner in the previous Office Action stating that "Applicant admits as well known in the art. . . that the principle cause of substrate noise generation is a change in voltage generated

when the source current of the digital circuits flowing through internal power-supply and ground wirings, ... the generation of noises largely depends on a change in the source current" is "irrelevant to modification of the teaching of Nagata et al. based on that of Shimazaki et al." The Examiner asserts that the cited text was to indicate that while the invention of Nagata is used to output a waveform indicating the substrate noise, since it is well known in the art that substrate noise is based upon the change in source current, one skilled in the art would have recognized the correspondence between the two values, further motivating the skilled artisan to make the combination.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure:

Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed-Signal IC Environment" teaches analysis with equivalent circuits to confirm that a charge transfer between the entire parasitic capacitance in digital circuits and an external supply through parasitic impedance to supply/return paths dominates the process, and the resultant retune bounce appears as the substrate noise. Nagata also teaches outputting a resultant waveform in the form of current or voltage.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
June 24, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800